Abstract

Packet processing circuitry comprises a processor and a look-up engine. For a first communication packet, the look-up engine transfers a first selector to a CAM and receives a corresponding first result from the CAM, retrieves a first context structure based on the first result and builds a summation block using the first context structure, transfers the summation block to the processor, writes a second selector to the CAM and receives a corresponding second result from the CAM, and writes the summation block to a memory location corresponding to the second result. For a second communication packet, the look-up engine transfers the second selector to the CAM and receives the corresponding second result from the CAM, retrieves the summation block based on the second result and transfers the summation block to the processor The processor receives and processes the summation block to control handling of the first and second communication packets.